Please amend Claims 1, 5, 7, and 12 and add new claim 16 as shown in this complete set of all pending Claims:

1. (currently amended) In a target processor, a trace apparatus comprising:

a trigger unit responsive to user and target processor state input signals, the trigger unit generating control signals in response to the input signals;

timing trace apparatus, the timing trace apparatus responsive to the control signals for selectively providing timing trace streams during secondary code execution, while continuing to provide timing trace streams during primary code execution;

program counter and data trace apparatus, the program counter and data trace apparatus responsive to the control signals ~~from the control apparatus~~ for selectively providing program counter and data trace streams during secondary code execution when the timing trace unit is providing ~~signal~~ timing trace streams during the secondary code execution; and

a test and debug port, the test and debug port adapted for coupling to a communication bus, the test and debug port receiving signals from and sending signals to a host processor unit.

2. (previously presented) The trace apparatus as recited in claim 1 wherein secondary code execution is a background or interrupt service routine code execution.

3. (currently amended) The trace apparatus as recited in claim 1 wherein the target processor [[is]] can have one of an unprotected pipeline and a protected pipeline.

4. (Original) The trace apparatus as recited in claim 1 further comprising a pipeline flattener, the pipeline flattener aligning the program counter address with the completion of the instruction, the pipeline flattener flushing instructions in response to a halt execution signal in an unprotected pipeline, the pipeline flattener halting operation in a protected pipeline.

5. (currently amended) The trace apparatus as recited in claim 1 wherein the target processor has three states, a primary code execution state, a secondary code execution state, and an execution halt state; and

wherein the trigger unit is responsive to the three states to selectively enable and disable the timing trace apparatus and the program counter and data trace apparatus in accordance with a current state of processor execution.

6. (Original) The trace apparatus as recited in claim 5 wherein the timing trace stream can be controllably enabled during an execution halt state.

7. (currently amended) A method of generating trace streams in a target processor for transmission to a host processor, the method comprising:

selecting one or more of a plurality of processor execution states, wherein tracing is enabled for the selected execution states and disabled for the non-selected execution states;

generating a timing trace stream in the target processor in response to preselected user and target processor input signals such that a timing trace stream is generated while the processor executes in a given execution state only when timing tracing is enabled for that execution state;

when the timing trace stream is being generated, generating a program counter and a data trace stream in response to predetermined user and target processor input signals, such that the program counter and the data trace stream is generated while the processor executes in a given execution state only when program counter and data tracing is enabled for that execution state; and

sending the trace streams to the host processing unit over a communication bus.

8. (Original) The method as recited in claim 7 further comprising including in the target processor input signals indicia of the state of the target processor, the target processor having a primary code execution state, a secondary code execution state and an execution halt state.

9. (Original) The method as recited in claim 7 further comprising including in the target processor input signals indicia indicating whether the target processor was in a protected pipeline mode of operation or in an unprotected pipeline mode of operation.

10. (Original) The method as recited in claim 7 further comprising including in the user input signals whether the timing trace was enabled during instruction execution halts.

11. (previously presented) The method as recited in claim 9 further comprising including in the user input signals identifying when the timing trace stream was enabled during the secondary code execution state.

12. (currently amended) A processing unit comprising:

a central processing unit, the central processing unit having three states of operation, a primary code execution state, a secondary code execution state and an execution halted state; and

trace generating apparatus including:

a program counter generation and a data trace stream generation unit, the program counter trace stream generation unit and the data trace generation unit responsive to control signals for generating the program counter and the data trace streams respectively;

a timing trace stream generation unit, the timing trace stream generation unit generating a timing trace stream in response to control signals;

a trigger unit responsive to user input signals and to central processing unit signals for generating first and second control signals controlling the timing trace generation unit and the program counter and data trace generation unit, wherein the trigger unit is operable to selectively enable and disable tracing by the program counter generation unit, by the data trace stream generation unit and by the timing trace stream generation unit in response to a current state of operation of the processing unit; and

a port for applying selected trace signal to a communication bus.

13. (Original) The processing unit as recited in claim 12 wherein first control signals enable the timing trace generation unit during the secondary code execution state.

14. (Original) The processing unit as recited in claim 13 wherein second control signals enable the timing trace generation device and the program counter and data trace generation units during the secondary code execution.

15. (Original) The processing unit as recited in claim 12 including indicia of a protected

pipeline mode of operation and of an unprotected mode of operation of the central processing unit are part of the central processing unit input signals.

16. (new) In a target processor, a trace apparatus comprising:

a trigger unit responsive to user and target processor state input signals, the trigger unit generating control signals in response to the input signals;

timing trace apparatus, the timing trace apparatus responsive to the control signals for selectively providing timing trace streams during secondary code execution;

program counter and data trace apparatus, the program counter and data trace apparatus responsive to the control signals for selectively providing program counter and data trace streams during secondary code execution when the timing trace unit is providing timing trace streams during the secondary code execution;

a pipeline flattener, the pipeline flattener aligning the program counter address with the completion of the instruction, the pipeline flattener flushing instructions in response to a halt execution signal in an unprotected pipeline, the pipeline flattener halting operation in a protected pipeline; and

a test and debug port, the test and debug port adapted for coupling to a communication bus, the test and debug port receiving signals from and sending signals to a host processor unit.